Notice of Allowability	Application No.	Applicant(s)	
	10/766,218	AKAHORI, HIDEKI	
	Examiner	Art Unit	
	MANSOUR M. SAID	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1/27/04*.

2. ☒ The allowed claim(s) is/are *1-11*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 1/27/04 & [illegible]4 1-13-06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

DETAILED ACTION

Allowable Subject Matter

1. **Claims 1-11 are allowed.**

2. The following is an examiner's statement of reasons for allowance: Claims 1-11 are allowed since certain key features of the claimed invention are not taught or fairly suggested by prior art. **In claim 1**, "a first synchronous delay circuit for adjusting a duty of said inputted clock and outputting it as a first clock, a second synchronous delay circuit for delaying said adjusted clock by a predetermined delay amount and outputting it as a second clock, a first holding circuit for holding and outputting said data in response to said first clock, and a second holding circuit for holding and outputting the data outputted from said first holding circuit in response to said second clock". **In claim 8**, "a first synchronous delay circuit for adjusting a duty ratio of the inputted clock and outputting it as a first clock, a second synchronous delay circuit for delaying said first clock by a predetermined delay amount and outputting it as a first delay clock, a first phase adjustment circuit for holding and outputting the data inputted based on said first clock and said first delay clock, a latch circuit for holding said held and outputted data in response to said first clock, a third synchronous delay circuit for readjusting the duty ratio of said first clock and supplying it as a second clock to a next-stage driver, a fourth synchronous delay circuit for delaying said second clock by the predetermined delay amount and outputting a second delay clock, and a second phase adjustment circuit for holding the data inputted based on said second clock and said second delay clock and outputting the held data to said next-stage driver". The closest prior art Iwata et al. (6,426,985 B1) teach a variable delay circuit includes a plurality of

delay circuits for delaying an input signal, and a selection circuit for selecting an output from one of the plurality of delay circuits in accordance with a selection signal, Chao et al. (6,667,580 B2) teach input/output clock phase adjustment circuitry for use with I/O buffer circuitry of an integrated circuit chip, however, singularly or in combination with other prior art, fail to anticipate or render the above underlined limitations obvious.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tamai et al. (6,697,041 B1) teach a display drive device including a plurality of cascade connected source driver chips for driving an LCD in accordance with an image data signal

Miyazawa (7,088,350 B2) teaches a display device includes a time-division-multiplexed driving of driver circuit.

Higuchi (2003/018,4354 A1) teaches a semiconductor integrated circuit.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mansour M. Said whose telephone number is 571-272-7679. The examiner can normally be reached on Monday through Thursday from 8:30-6:00 P.M. The

examiner can also be reached on alternate Friday from 8:30 a.m. to 5:00 p.m. EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe whose telephone number is 571-272-7681.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: 571-273-8300 (for Technology Center 2600 only)

Hand-delivered responses should be brought to the Customer Service Window at the Randolph Building, 401, Dulany Street, Alexandria, VA 22314.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mansour M. Said

9/13/06

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600